Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **Clear**
2. **Clock**
3. **A**
4. **B**
5. **C**
6. **D**
7. **Enable P**
8. **GND**
9. **Load**
10. **Enable T**
11. **QD**
12. **QC**
13. **QB**
14. **QA**
15. **Ripple Carry Output**
16. **Vcc**

**6 5 4 3**

**2**

**1**

**16**

**15**

**7**

**8**

**9**

**10 11 12 13 14**

**163**

**MASK**

**REF**

**LS**

**.059”**

**.059”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 163**

**APPROVED BY: DK DIE SIZE .059” X .059” DATE: 8/29/22**

**MFG: MOTOROLA THICKNESS .015” P/N: 54LS163A**

**DG 10.1.2**

#### Rev B, 7/19/02